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TiN and TaN diffusion barriers in copper interconnect technology: Copper Interconnect Technology, Bellingham, WA: SPIE Press, 2001). 3. J. Li and J.W. Mayer, Mater.

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chips using this technology can have smaller metal components, Damascene processes generally form and fill a single feature with copper per Damascene stage.

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Apr 24, 2013 The rapid development of 3D chips presents new challenges still to be overcome in stacking, scaling, and performance. SPIE Advanced Lithography Symposium

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## **Brad smith | linkedin**

View Brad Smith's professional profile on LinkedIn. transferred the 90nm copper interconnect into volume SPIE -- Multi-level Interconnect Technology September

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Copper interconnect technology. [Christoph Steinbruechel; SPIE Optical Engineering Press, " Tutorial texts in optical engineering ; "

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Method of forming barrier layers for damascene interconnects "Copper Chip" Technology, SPIE Conference on Multilevel Copper interconnect structures and

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Christoph Steinbruechel; Copper interconnect technology is expected to be a key component in the This text examines the role of copper in future

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The 17th annual International Interconnect Technology Conference (IITC) In ordinary conductors such as copper, 2015 SPIE Advanced Lithography EUVL

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